



PATENT
Attorney Docket No. 400762/AOYAMA

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

SUZUKI et al.

Application No. 09/613,749

Art Unit: 2814

Filed: July 11, 2000

Examiner: A. Rao

For: **FIELD EFFECT TRANSISTOR
STRUCTURE WITH BENT GATE**

RECEIVED
JAN 29 2003
TECHNOLOGY CENTER 2800

**PENDING CLAIMS AFTER AMENDMENTS
MADE IN RESPONSE TO OFFICE ACTION DATED OCTOBER 4, 2002**

18. A semiconductor device comprising:

a compound semiconductor substrate having a first surface and a second surface, the compound semiconductor substrate being electrically isotropic in two mutually orthogonal directions;

first, second, and third active regions on the first surface of the substrate, the first and second active regions being separated by a first insulating region and the second and third active regions being separated by a second insulating region;

a first semiconductor element including

first, second, and third channel regions serially connected, adjacent channel regions having width directions essentially perpendicular to each other,

a first source electrode and a first drain electrode, adjacent to the first, second, and third channel regions and opposing each other with the first, second, and third channel regions therebetween, and in ohmic contact with the first, second, and third active regions, and

a first gate electrode disposed on the first, second, and third channel regions and along the first source electrode and the first drain electrode, and bent at first and second bending positions; and

a second semiconductor element on the first, second, and third active regions adjacent to the first semiconductor element, including

fourth, fifth, and sixth channel regions serially connected, adjacent channel regions having width directions essentially perpendicular to each other, the fourth, fifth, and sixth channel regions being adjacent to the first, second, and third channel regions, respectively, with one of the first source electrode and the first drain electrode therebetween,

a second source electrode and a second drain electrode in ohmic contact with the first, second, and third active regions, one of the second source electrode and the second drain electrode and opposing the first drain electrode or the first source electrode across the fourth, fifth, and sixth channel regions, and

a second gate electrode on the fourth, fifth, and sixth channel regions and along one of the second source electrode and the second drain electrode, and bent at third and fourth bending positions, wherein the first insulating region is under the first and third bending positions of the first and second gate electrodes, and the second insulating region is under the second and fourth bending positions of the first and second gate electrodes.

19. The semiconductor device according to claim 18 wherein the first source electrode is connected to a conductive film on the second surface of the semiconductor substrate through a via-hole in the first source electrode.

20. The semiconductor device according to claim 18 wherein the first bending position of the first gate electrode and the third bending position of the second gate electrode lie on a straight line substantially parallel to a longer side of the first, second, and third active regions.

21. The semiconductor device according to claim 18, wherein the first gate electrode is bent in opposite directions at the first and second bending positions, and wherein the second gate electrode extends substantially at a uniform spacing from the first gate electrode.

22. The semiconductor device according to claim 18, wherein the first gate electrode and second gate electrode share one of the first source electrode and the first drain electrode.

23. The semiconductor device according to claim 18 wherein the first gate electrode is bent at right angles at each of the first and second bending positions.

24. The semiconductor device according to claim 23 wherein the second gate electrode is bent at right angles at each of the third and fourth bending positions.

25. The semiconductor device according to claim 18, wherein an angle between the width direction of the first gate electrode and a longer side of the first, second, and third active regions is essentially 45°.